REMARKS

Reconsideration of this application is respectfully requested.

The Examiner rejected claims 1-11 and 18-19. Claims 1-11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,867,430 of Chen ("Chen") and "applicant admitted prior art" ("AAPA"), in view of U.S. Patent 6,182,189 of Alexis ("Alexis"). Claims 18-19 are rejected under 35 U.S.C. § 102(b) as being anticipated by Chen.

Applicants submit that Claim 1 is patently distinguished over Chen and AAPA, in view of Alexis. Claim 1 includes the limitations:

> a memory array having a first plane, a second plane, a third plane, and a fourth plane, wherein a first partition of the memory array comprises one of the planes and a second partition of the memory array comprises the remaining planes, wherein a write operation is performed on the first partition and a read operation is concurrently performed on the second partition; and
>
> a status register coupled to the memory array, wherein the status register provides status information of the first plane, the second plane, the third plane, and the fourth plane.

(Claim 1) (emphasis added).

Chen discloses a memory device that is divided into two or more banks... The output data for each bank can be communicated to a read sense amplifier or a verify sense amplifier. (Chen, column 2, lines 1-8).

AAPA discloses that each partition of a memory array has a designated status register.

Alexis discloses in Figure 2 a serial control logic 280 to control the serial coupling of the verify sense amp 150 to different memory locations to be verified

by the write plane. (Alexis, column 6, lines 32-35).

It is respectfully submitted that Chen and AAPA do not teach or suggest a combination with Alexis and that Alexis does not teach or suggest a combination with Chen and AAPA. It would be impermissible hindsight based on applicants' own disclosure to incorporate the memory device of Chen and the designated status registers of AAPA into the circuit of Alexis.

Moreover, such a combination would still lack a status register that provides status information of a first plane, a second plane, a third plane, and a fourth plane. The Examiner alleges that Alexis teaches a status register coupled to a memory array. (01/29/04 Office Action, page 4, lines 18-21). The Examiner identified element 150 in Figure 2 of Alexis as a status register. Thus, the Examiner concluded that the "status register" 150 of Alexis provides status information of the first plane, the second plane, the third plane, and the fourth plane. Applicants respectfully disagree. Figure 2 and the specification of Alexis clearly state that element 150 is a verify **sense amplifier**. It is well known to those having ordinary skill in the art that a sense amplifier is not a status register or the functional equivalent of a status register.

Furthermore, even if Chen, AAPA, and Alexis did disclose a status register that is coupled to a memory array, Chen, AAPA, and Alexis fail to disclose a single status register that is used to provide status information of a first plane, a second plane, a third plane, and a fourth plane of the memory array as set forth in Claim 1.

Given that Claims 2-5 depend from Claim 1, applicants submit that Claims

2-5 are patently distinguished over the references cited by the Examiner.

Applicants submit that Claim 6 is patently distinguished over Chen and AAPA, in view of Alexis. Claim 6 includes the limitations:

> dividing the memory array into n planes, wherein n is an integer greater than two;
> defining a write partition, wherein the write partition is a single plane of the memory array;
> defining a read partition, wherein the read partition is made up of all of the remaining n planes of the memory array; and
> providing the status of the read partition and the write partition of the memory array with a single status register.

(Claim 6) (emphasis added).

Chen discloses a memory device that is divided into two or more banks. (Chen, column 2, lines 1-2). While one bank is busy with the program or erase operation, the other bank can be accessed for reading data. (Chen, column 2, lines11-13).

AAPA discloses that each partition of a memory array has a designated status register.

Alexis discloses in Figure 2 a serial control logic 280 to control the serial coupling of the verify sense amp 150 to different memory locations to be verified by the write plane. (Alexis, column 6, lines 32-35).

It is respectfully submitted that Chen and AAPA do not teach or suggest a combination with Alexis and that Alexis does not teach or suggest a combination with Chen and AAPA. It would be impermissible hindsight based on applicants' own disclosure to incorporate the memory device of Chen and the designated status registers of AAPA into the circuit of Alexis.

Moreover, such a combination would still lack providing the status of the read partition and the write partition of the memory array with a single status register. The Examiner alleges that Alexis teaches a status register coupled to a first and second plane which are included in a memory array. (01/29/04 Office Action, page 6, lines 12-14). The Examiner identified element 150 in Figure 2 of Alexis as a status register. Thus, the Examiner concluded that the "status register" 150 of Alexis provides status information of the first plane, the second plane, the third plane, and the fourth plane. Applicants respectfully disagree. Figure 2 and the specification of Alexis clearly state that element 150 is a verify **sense amplifier**. It is well known to those having ordinary skill in the art that a sense amplifier is not a status register or the functional equivalent of a status register.

Furthermore, even if Chen, AAPA, and Alexis did disclose a status register that is coupled to a memory array, Chen, AAPA, and Alexis fail to disclose providing the status of the read partition and the write partition of the memory array with a single status register as set forth in Claim 6.

Given that Claims 7-11 depend from Claim 6, applicants submit that Claims 7-11 are patentably distinguished over the references cited by the Examiner.

Applicants submit that Claim 18 is not anticipated under 35 U.S.C. § 102(b) by Chen. Claim 18 includes the limitation:

> means for partitioning a memory array into a fixed first partition and a variable second partition to enable multiple operations to be performed on the memory array at the same time; and

means for monitoring the operations performed on the memory array.

(Claim 18) (emphasis added).

In contrast, Chen discloses a memory device that is divided into two or more banks. (Chen, column 2, lines 1-2). Chen does not disclose partitioning a memory array into a **fixed** first partition and a **variable** second partition. The Examiner alleges that Chen discloses a variable second partition because "the rest of banks are accessed by the read operations." 01/29/04 Office Action, page 3, lines 1-2). This, however, is a misstatement of Chen. Chen states that "while one bank is busy with the program or erase operation, the **other bank** can be accessed for reading data. Chen does not mention reading from more than one bank. As a result, applicants respectfully submit that Chen fails to disclose a variable second partition as interpreted by the Examiner.

Further, Chen discloses a memory device that receives an address input and includes a state machine **performing** the embedded methods of erasing and programming. (Chen, column 2, lines 24-26). Chen does not disclose **monitoring** the operations performed on a memory array as set forth in Claim 18.

Given that Claim 19 depends from Claim 18, applicants submit that Claim 19 is not anticipated by Chen.

Respectfully submitted,

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